What is Claimed is:

1. An apparatus for modulating and demodulating signals transmitted and received via an electronically steerable phased array antenna comprising a plurality of antenna elements, the apparatus comprising:

a baseband modulator configured to modulate signals to be transmitted via the phased array antenna;

a baseband demodulator configured to demodulate signals received via the phased array antenna; and

a shared baseband processor configured to receive baseband signals including the modulated signals from said baseband modulator and the signals received via the phased array antenna which are destined for said baseband demodulator, said shared baseband processor adjusting phases of the baseband signals to jointly account for beamforming phase rotation of individual antenna elements and carrier phase rotation, and adjusting amplitudes of the baseband signals to jointly perform power control and antenna element beam scaling.

2. The apparatus of claim 1, wherein said baseband signals received by said shared baseband processor are time multiplexed, and said shared baseband processor operates on said baseband signals on a time-slot-by-time-slot basis.

3. The apparatus of claim 1, wherein said baseband modulator receives data symbols from a plurality of user channels and supplies to said shared baseband processor a time-multiplexed stream of modulated data symbols from said plurality of user channels.

4. The apparatus of claim 3, wherein, for each input data symbol, said baseband modulator generates a plurality of modulated data symbols in the time-multiplexed stream respectively corresponding to the plurality of antenna elements.

5. The apparatus of claim 1, wherein said shared baseband processor comprises:

a numerically controlled oscillator configured to generate a stream of carrier phases for baseband signals of each of a plurality of user channels in a time-multiplexed manner;

a beamforming phase rotator configured to generate a stream of beam rotation phases corresponding to individual antenna elements for each of the plurality of user channels in a time-multiplexed manner;

a phase adder configured to sum the beam rotation phases and the carrier phases to produce a time-multiplexed stream of combined phase adjustments; and

a complex multiplier configured to adjust phases of a time-multiplexed stream of baseband signals corresponding to the plurality of user channels in accordance with the combined phase adjustments.

6. The apparatus of claim 5, wherein said combined phase adjustments index a sine/cosine lookup table which supplies multiplicands to said complex multiplier.

7. The apparatus of claim 1, wherein said shared baseband processor comprises a multiplier which performs complex multiplication on baseband signals relating to a plurality of user channels in a time-multiplexed manner.

8. The apparatus of claim 1, wherein said shared baseband processor comprises a multiplier which performs complex multiplication on baseband signals associated with a plurality of individual antenna elements in a time-multiplexed manner.

9. The apparatus of claim 1, wherein said shared baseband processor comprises a beam scaling and power control processor configured to generate a time-multiplexed stream of gain control signals for baseband signals corresponding to individual antenna elements for each of a plurality of user channels, the gain control signals jointly accounting for power control and antenna element beam scaling; and

a multiplier configured to adjust amplitudes of a time-multiplexed stream of baseband signals corresponding to the plurality of user channels in accordance with the gain control signals.

10. The apparatus of claim 1, further comprising:

a baseband beamformer configured to receive time-multiplexed baseband signals from said shared baseband processor corresponding to individual antenna elements, said baseband processor forming a combined signal from said time-multiplex baseband signals.

11. The apparatus of claim 1, further comprising:

a plurality of digital down-converters respectively down-converting digitized signals

received from the plurality of antenna elements to produce parallel streams of sampled baseband signals; and

a multiplexer receiving the parallel streams of sampled baseband signals and supplying a time-multiplexed stream of the sampled baseband signals to said shared baseband processor.

12. The apparatus of claim 11, wherein said plurality of digital down-converters perform decimation to reduce a sampling rate of the digitized signals.

13. The apparatus of claim 11, wherein said plurality of digital down-converters separately down-convert digitized signals for each antenna element for each of a plurality of frequency channels.

14. The apparatus of claim 1, further comprising:

a demultiplexer receiving a time-multiplexed stream of baseband signals from said shared baseband processor and generating parallel streams of baseband signals corresponding to the plurality of antenna elements; and

a plurality of digital up-converters respectively up-converting the parallel streams of baseband signals to produce a plurality of digitized intermediate frequency signals corresponding to the plurality of antenna elements.

15. The apparatus of claim 14, wherein said plurality of digital up-converters perform interpolation to increase a sampling rate of the digitized intermediate frequency signals.

16. The apparatus of claim 14, wherein said plurality of digital up-converters separately up-convert baseband signals for each antenna element for each of a plurality of frequency channels.

17. The apparatus of claim 1, wherein signals are transmitted and received using time division duplex, said apparatus further comprising switching elements to selectively connect said shared baseband processor to said baseband modulator and front-end transmit circuitry for signal transmission and to said baseband demodulator and front-end receive circuitry for signal reception.

18. The apparatus of claim 1, wherein said apparatus employs time division multiple access (TDMA) to transmit and receive signals.

19. The apparatus of claim 1, wherein said apparatus employs frequency division multiple access (FDMA) to transmit and receive signals.

20. The apparatus of claim 1, wherein said apparatus is a field programmable gate array (FPGA).

21. The apparatus of claim 1, wherein the apparatus is implemented via a very large scale integration (VLSI) circuit or an application specific integrated circuit (ASIC).

22. The apparatus of claim 1, wherein said apparatus is a modem.

23. The apparatus of claim 1, wherein said apparatus is a transceiver.

24. The apparatus of claim 1, wherein said apparatus is a basestation transceiver.